

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

Do-Hyung Kim et al.

METHOD OF FORMING A DEVICE ISOLATION TRENCH IN AN INTEGRATED CIRCUIT DEVICE
 Attorney Docket No. 4591-226/Application No. Not yet filed

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Fig. 1

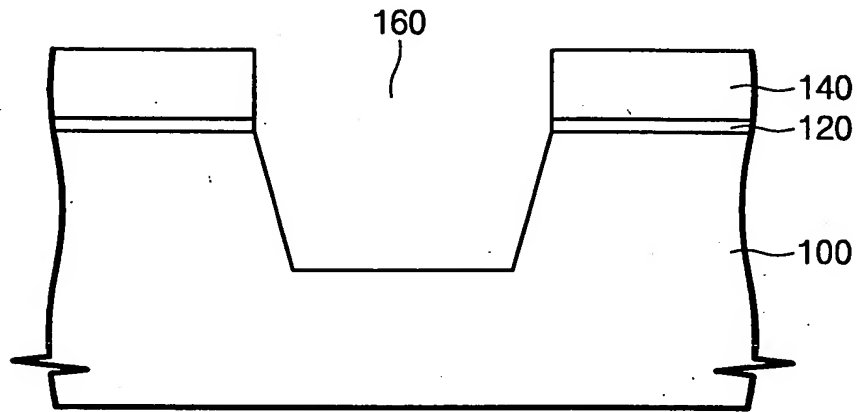
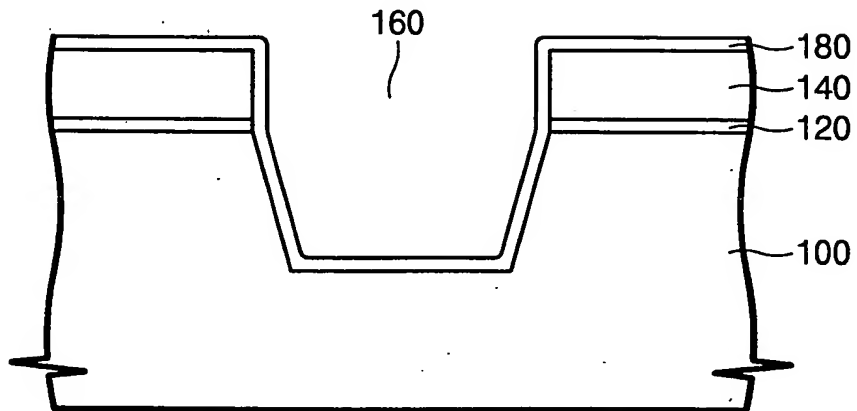


Fig. 2



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Fig. 3

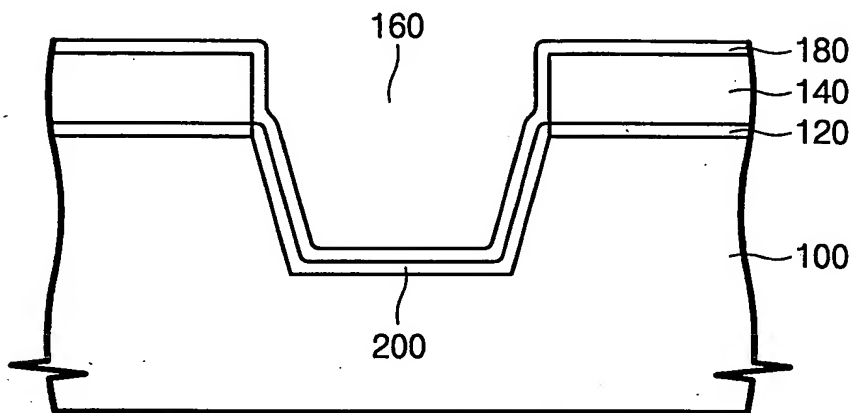
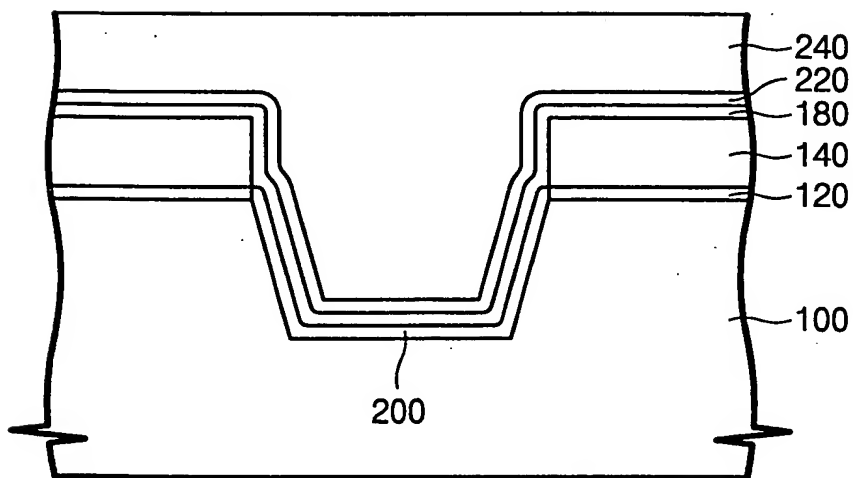


Fig. 4



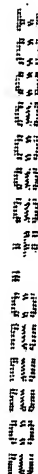
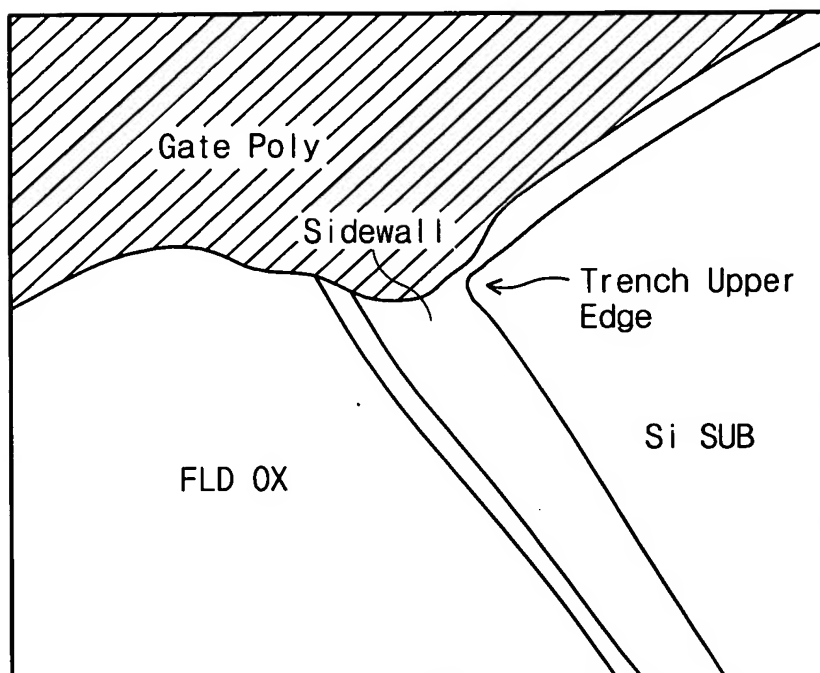


Fig. 8

(Prior Art)



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Fig. 9

(Prior Art)

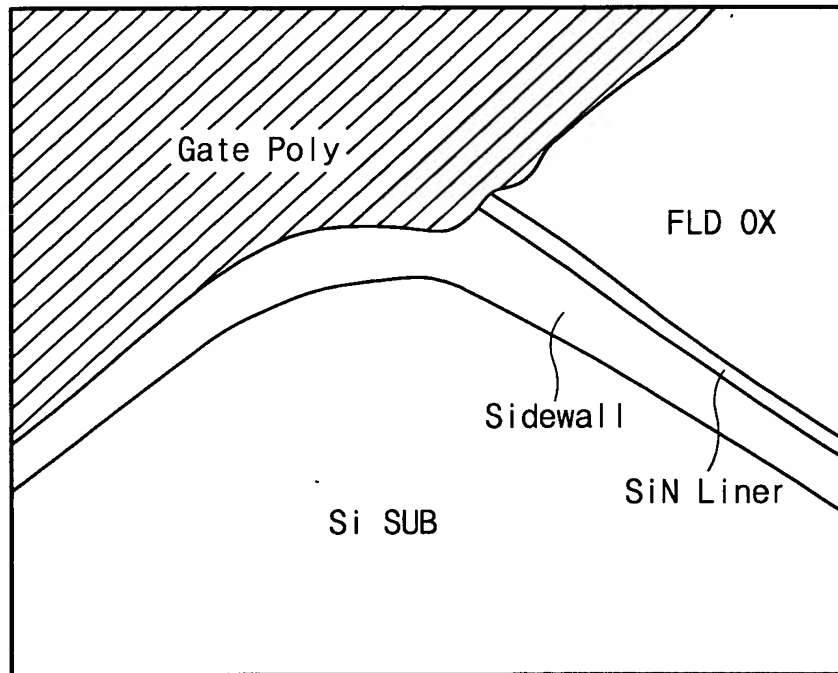


FIG. 9 is a cross-sectional view of a semiconductor device structure, showing a silicon substrate (Si SUB) with a silicon nitride liner (SiN Liner) and a gate poly (Gate Poly) layer. A field oxide (FLD OX) layer is formed on the right side of the gate poly, and a sidewall is formed on the right side of the gate poly, extending from the field oxide layer down to the silicon nitride liner layer.

Fig. 10

(Prior Art)

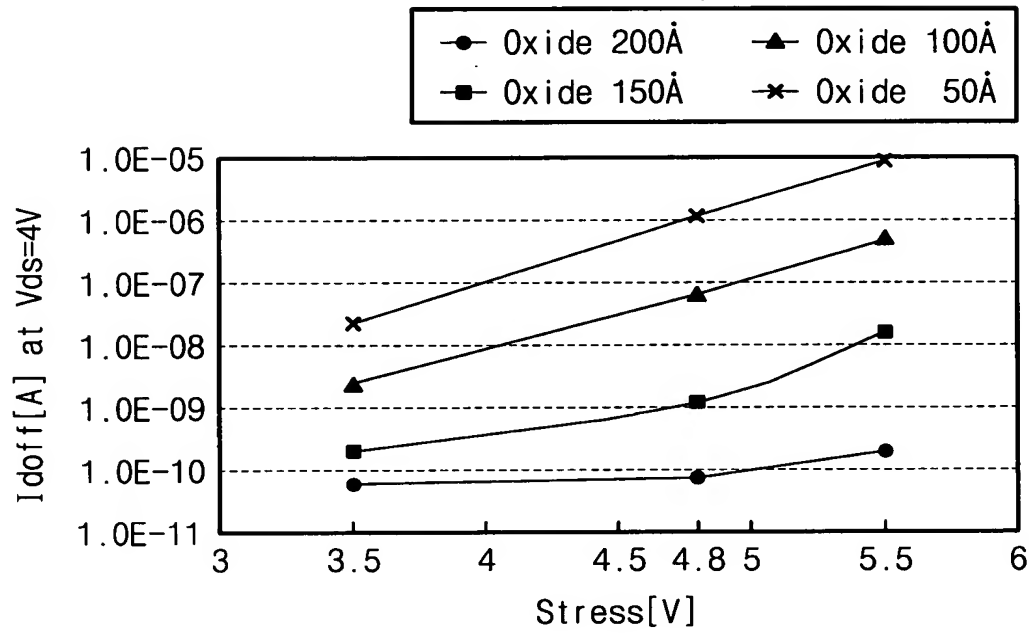


Fig. 11

